ABSTRACT OF THE DISCLOSURE

A dynamic logic register including a dynamic circuit, a delayed inverter, a latching circuit, and a keeper circuit. The dynamic circuit pre-charges a pre-charged node while a clock signal is low and evaluates a logic function to control the state of the pre-charged node when the clock goes high. The delayed inverter provides an inverted and delayed clock. The latching circuit controls the state of an output node based on the pre-charged node during an evaluation period beginning when the clock goes high and ending when the inverted delayed clock next goes low. The latching circuit presents a tri-state condition to the output node and the keeper circuit maintains the state of the output node between evaluation periods. The register is very fast with zero setup and short data-to output-time, and may be used between stages in a pipeline system.